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IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An apparatus to provide data based in part on a justification command, the apparatus comprising:

processor logic to selectively provide a justification command and data from an input signal;

a clock source to provide a first clock signal, wherein the clock source selectively modifies a phase of the first clock signal in response to the justification command; and

an elastic store device to selectively transfer the data based in part on the first clock signal,

wherein the clock source comprises first, second, and third clock sources to respectively provide the first, a second, and a third clock signals; a transform device to modify the phase of the first clock signal in response to the justification command, to update a phase account to account for a phase impact of a positive justification command, and to update the phase account according to an amount of clock signal phase shift adjustment; and a phase comparator to modify the phase of the second clock signal based on a phase comparison of the first and third clock signals.

2. (Currently Amended) The apparatus of Claim of 1, wherein the clock source is to selectively add a cycle to the first clock signal in response to a negative justification command and a phase account ~~being low enough~~ value to allow a phase adaptation.

3. (Currently Amended) The apparatus of Claim 1, wherein the clock source is to selectively remove a cycle from the first clock signal in response to a positive justification command and a phase account ~~being enough~~ value to allow a phase adaptation.

4. (Previously Presented) The apparatus of Claim 1, wherein the processor logic is to perform forward error correction decoding in accordance with ITU-T G.975.

5. (Previously Presented) The apparatus of Claim 1, wherein the processor logic is to identify the justification command in compliance with ITU-T G.709.

6. (Original) The apparatus of Claim 1, wherein the input signal comprises an OTN frame.

7. (Canceled) ~~The apparatus of Claim 1, wherein the clock source comprises:~~

~~a first clock source to provide the first clock signal;~~

~~a second clock source to provide a second clock signal;~~

~~a third clock source to provide a third clock signal based on the second clock signal;~~

~~a transform device to selectively modify the phase of the first clock signal in response to the justification command; and~~

~~a phase comparator to selectively modify the phase of the second clock signal based on phase comparisons between the first and third clock signals.~~

8. (Currently Amended) The apparatus of Claim [[7]] 1, wherein the transform device is to selectively update a phase account to account for a phase impact of a negative justification command in response to a negative justification command.

9. (Currently Amended) The apparatus of Claim 8, wherein the transform device is to selectively update the phase account according to an amount of clock signal phase shift adjustment in response to a first value of the phase account ~~being low enough~~ to allow a phase adaptation.

10. (Currently Amended) The apparatus of Claim 9, wherein the transform device is to selectively wait for a next justification command in response to a second [[the]] phase account value ~~not being low enough~~ to allow a phase adaptation.

11. (Canceled) ~~The apparatus of Claim 7, wherein the transform device is to selectively update a phase account to account for a phase impact of a positive justification command in response to a positive justification command.~~

12. (Currently Amended) ~~The apparatus of Claim 11, wherein the transform device is to selectively update the phase account according to an amount of clock signal phase shift adjustment in response to the phase account being enough to allow a phase adaptation.~~

13. (Currently Amended) The apparatus of Claim [[12]] 1, wherein the transform device is to selectively wait for a next justification command ~~in response to the phase account not being enough to allow a phase adaptation~~.

14. (Currently Amended) The apparatus of Claim [[7]] 1, wherein the clock source is to selectively maintain a ratio of the first clock signal to the third clock signal as approximately one in response to the justification command.

15. (Previously Presented) An apparatus to provide at least one justification command comprising:

an elastic store device to selectively transfer data based on a first clock signal;

a justification source to selectively provide a justification command based on a phase comparison between second and third clock signals;

a transform device to selectively modify the phase of the second clock signal in response to the justification command; and

a wrapper device to selectively combine the justification command with the data based on the first clock signal and to provide the combination.

16. (Currently Amended) The apparatus of Claim 15, wherein the transform device is to selectively add a cycle to the second clock signal in response to a negative justification command and a phase account ~~being low enough~~ value to allow a phase adaptation.

17. (Currently Amended) The apparatus of Claim 15, wherein the transform device is to selectively remove a cycle from the second clock signal in response to a positive justification command and a phase account ~~being enough~~ value to allow a phase adaptation.

18. (Original) The apparatus of Claim 15, wherein the wrapper device is to perform forward error correction encoding in accordance with ITU-T G.975.

19. (Original) The apparatus of Claim 15, wherein the wrapper device is to provide the combination in accordance with ITU-T G.709.

20. (Original) The apparatus of Claim 15, wherein the second clock signal is based on the first clock signal.

21. (Previously Presented) The apparatus of Claim 15, wherein the justification source is to selectively provide a positive justification command in response to the phase comparison exceeding a threshold.

22. (Previously Presented) The apparatus of Claim 15, wherein the justification source is to selectively provide a negative justification command in response to the phase comparison being less than a threshold.

23. (Previously Presented) The apparatus of Claim 15, further comprising a phase comparator to selectively provide the phase comparison, wherein the phase comparison is between the second and third clock signals.

24. (Previously Presented) The apparatus of Claim 15, wherein the transform device is to selectively update a phase account to account for a phase impact of a negative justification command in response to a negative justification command.

25. (Currently Amended) The apparatus of Claim 24, wherein the transform device is to selectively update the phase account according to an amount of clock signal phase shift adjustment in response to a first value of the phase account ~~being low enough~~ to allow a phase adaptation.

26. (Currently Amended) The apparatus of Claim 25, wherein the transform device is to selectively wait for a next justification command in response to a second value of the phase account ~~not being low enough~~ to allow a phase adaptation.

27. (Previously Presented) The apparatus of Claim 15, wherein the transform device is to selectively update a phase account to account for a phase impact of a positive justification command in response to a positive justification command.

28. (Currently Amended) The apparatus of Claim 27, wherein the transform device is to selectively update the phase account according to the amount of clock signal phase shift adjustment ~~in response to the phase account being enough to allow a phase adaptation~~.

29. (Currently Amended) The apparatus of Claim 28, wherein the transform device is to selectively wait for a next justification command ~~in response to the phase account not being enough to allow a phase adaptation~~.

30. (Original) The apparatus of Claim 15, wherein the transform device is to selectively maintain a ratio of the second clock signal to the third clock signal as approximately one in response to the justification command.

31. (Currently Amended) A method to provide data based in part on a justification command comprising:

selectively extracting a justification command and data from an input signal;

selectively modifying a phase of a first clock signal in response to the justification command, wherein the justification command is provided based on a phase comparison between second and third clock signals; [[and]]

selectively transferring the data based in part on the first clock signal;

selectively modifying the phase of the second clock signal in response to the justification command; and

selectively combining the justification command with the data based on the first clock signal.

32. (Original) The method of Claim 31, wherein the modifying comprises selectively adding a cycle to the first clock signal in response to a negative justification command and the number of accounted-for bits being low enough to allow a phase adaptation.

33. (Original) The method of Claim 31, wherein the modifying comprises selectively removing a cycle from the first clock signal in response to a positive justification command and the number of accounted-for bits being enough to allow a phase adaptation.

34. (Original) The method of Claim 31, wherein the input signal comprises an OTN frame.

35. (Previously Presented) A method to provide a justification command comprising:

selectively transferring data based on a first clock signal;

selectively providing a justification command based on a phase comparison between second and third clock signals;

selectively modifying the phase of the second clock signal in response to the justification command; and

selectively combining the justification command with the data based on the first clock signal.

36. (Original) The method of Claim 35, wherein the modifying comprises selectively adding a cycle to the second clock signal in response to a negative justification command and a phase account being low enough to allow a phase adaptation.

37. (Original) The method of Claim 35, wherein the modifying comprises selectively removing a cycle from the second clock signal in response to a positive justification command and a phase account being enough to allow a phase adaptation.

38. (Currently Amended) A system to provide data based in part on a justification command comprising:

an interface;

a data processor communicatively coupled with the interface and to selectively provide a justification command and data from an input signal;

a clock source to provide a first clock signal, wherein the clock source selectively modifies a phase of the first clock signal in response to the justification command; and

an elastic store device to selectively transfer the data based in part on the first clock signal,

wherein the clock source comprises first, second, and third clock sources to respectively provide the first, a second, and a third clock signals; a transform device to update a phase account to account for a phase impact of a positive justification command and to update the phase account according to an amount of clock signal phase shift adjustment; and a phase comparator to modify the phase of the second clock signal based on a phase comparison of the first and third clock signals.

39. (Original) The system of Claim 38, wherein the interface is compatible with XAUI.

40. (Original) The system of Claim 38, wherein the interface is compatible with IEEE 1394.

41. (Original) The system of Claim 38, wherein the interface is compatible with PCI.

42. (Original) The system of Claim 38, wherein the data processor is to perform media access control in compliance with IEEE 802.3.

43. (Original) The system of Claim 38, wherein the data processor is to perform optical transport network de-framing in compliance with ITU-T G.709.

44. (Original) The system of Claim 38, wherein the data processor is to perform forward error correction processing in compliance with ITU-T G.975.

45. (Original) The system of Claim 38, further comprising a switch fabric coupled to the interface.

46. (Original) The system of Claim 38, further comprising a packet processor coupled to the interface.

47. (Original) The system of Claim 38, further comprising a memory device coupled to the interface.

48. (Previously Presented) A system to provide a justification command comprising:

an interface;

an elastic store device communicatively coupled with the interface and to selectively transfer data in response to a first clock signal;

a justification source to selectively provide a justification command based on a phase comparison between second and third clock signals;

a transform device to selectively modify the phase of the second clock signal in response to the justification command; and

a wrapper device to selectively combine the justification command with the data based on the first clock signal and to provide the combination; and

a data processor communicatively coupled with the interface and the wrapper device.

49. (Original) The system of Claim 48, wherein the interface is compatible with XAUI.

50. (Original) The system of Claim 48, wherein the interface is compatible with IEEE 1394.

51. (Original) The system of Claim 48, wherein the interface is compatible with PCI.

52. (Cancelled)

53. (Previously Presented) The system of Claim 48, wherein the data processor is to perform optical transport network framing in compliance with ITU-T G.709.

54. (Original) The system of Claim 48, wherein the data processor is to perform forward error correction processing in compliance with ITU-T G.975.

55. (Original) The system of Claim 48, further comprising a switch fabric coupled to the interface.

56. (Original) The system of Claim 48, further comprising a packet processor coupled to the interface.

57. (Original) The system of Claim 48, further comprising a memory device coupled to the interface.